



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/519,867

12/30/2004

Fan Yung Ma

2004 LW 2463 US

9311

48154

7590

11/14/2005

SLATER & MATSIL LLP
17950 PRESTON ROAD
SUITE 1000
DALLAS, TX 75252

EXAMINER

HILTUNEN, THOMAS J

ART UNIT

PAPER NUMBER

2816

DATE MAILED: 11/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/519,867

Applicant(s)

MA, FAN YUNG

Examiner

Thomas J. Hiltunen

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1,2 and 4-8 is/are rejected.
- 7) ☒ Claim(s) 3 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12/30/04 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. ____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>12/30/04, 5/16/05</u> | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

Drawings

The drawings are objected to because they do not have the required bubbles to indicate connections between elements or interconnect lines in Fig. 2 and Fig. 3. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112, second paragraph

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 4-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 4 is misdescriptive, it is not understood how the recited components of claim 4 can constitute a "microprocessor". Claims 5-7 are rejected as to not overcoming the indefiniteness of claim 4.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 rejected under 35 U.S.C. 102(b) as being anticipated by Winebarger (USPN 4,260,907).

With respect to claim 1 Winebarger discloses in Fig. 2, a detection circuit for monitoring a supply voltages the circuit comprising:

"a comparator (46) for generating a shortfall signal indicative of a shortfall of the supply voltage (V+ at node 12 is supplied to node 42 of 46 through R1) in relation to a reference voltage (voltage at the - terminal of 46 at node 44), and an integrator for time-integrating the shortfall signal to form an integrated signal (R4 and C2 form an integrator), wherein the output of the integrator is used to generate a reset signal for

Art Unit: 2816

resetting a microprocessor (it can be seen that the output of the integrator is supplied as a power-on reset signal at the output of inverter 60)."

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Winebarger (4,260,907). Winebarger teaches, in Fig 2 the circuit recited in claim 4. Winebarger does not explicitly teach the use of the circuit in Fig. 3 with a microprocessor. However, Winebarger discloses (in Col. 1 lines 6-17) that the invention "lies in the field of electronic equipment", and more specifically electronic equipment in which problems arise when "the power supply to the equipment fails". Winebarger also discloses that this detection circuit can be used in electronic equipment where "there are one or many, flip flops, adders, registers, counters, etc." It would be obvious for one skilled in the art at the time of the invention to include microprocessors in this "electronic equipment" category, because microprocessors are commonly composed of the above list of "electronic equipment". Additionally, a microprocessor would be included in the above mentioned "electronic equipment". Thus, it is obvious that Winebarger teaches the use of the above reset circuit to reset microprocessors.

It would have been *prima facie* obvious to one of ordinary skill in the art at the time the invention was made to reset a microprocessor with Winebargers above recited reset circuit for the purpose of having a simply a simply constructed power-on reset circuit that resets when the supply voltage drops below a certain level (See Col. 2 lines 5-15). One skilled in the art would have been motivated to combine the circuit of Winebarger with a microprocessor with a reasonable expectation of success.

With respect to claim 4, Winebarger as modified above discloses in Fig. 2, A circuit comprising:

"a comparator (46) for generating a shortfall signal indicative of a shortfall of the supply voltage (V+ at node 12 is supplied to node 42 of 46 through R1) in relation to a reference voltage (voltage at the – terminal of 46 at node 44), and an integrator for time-integrating the shortfall signal to form an integrated signal (R4 and C2 form an integrator), wherein the output of the integrator is used to generate a reset signal for resetting a microprocessor (it can be seen that the output of the integrator is supplied as a power-on reset signal at the output of inverter 60), and

reset means arranged to receive the reset signal output by the UVD circuit and according to its value to initiate a reset of the microprocessor." (Since it is obvious to use the reset signal of Winebarger with a microprocessor, it is inherent that the microprocessor has a means to receive the reset signal, which is being used to reset the microprocessor).

With respect to claim 5, Winebarger as modified above discloses in Fig. 2, a method including:

“generating a shortfall signal indicative of a shortfall of the supply voltage in relation to a reference voltage (46 outputs at 58 a signal that detects if the signal ant 42 of 46 is lower than the signal at 44 of 46), time-integrating the shortfall signal to form an integrated signal (R4 and C2 act as integrator, which integrates the output of 58), and generating a reset signal using the shortfall signal, wherein the reset signal is for resetting a microprocessor (as explained above it would be obvious to use the circuit of Fig. 2 to reset a microprocessor).”

With respect to claim 6, Winebarger as modified above discloses in Fig. 2, the method of claim 5 and further comprising resetting the microprocessor with the reset signal. (as disclosed above it is obvious to use the reset signal to reset the microprocessor.)”

Claims 1-2, and 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshimura (5,629,642) in view of Woods (USPN 6,259,285). Yoshimura teaches, in Fig. 1 a comparator detects a shortfall in a supply by receiving a supply voltage and a reference voltage. The output of the comparator is input to a discriminator circuit, and a delay circuit, which is used to prevent a reset when the power supply voltage is instantaneously decreased. It is used to delay the comparators signal by a prescribed amount of time. (See Col. 1 lines 51-58). This delay circuit also outputs a signal to the discriminator. The discriminator then outputs a reset signal based on the inputs of the delay and comparator circuits. Yoshimura does not teach an integrator circuit receiving the output of the comparator. Woods teaches, in Fig. 1 a delay circuit that integrates

signals input to it. Woods' delay circuit as disclosed is used in a reset circuit that detects power loss. Additionally, Woods' delay circuit is used to "filter out rapid perturbations in the power supply voltage" (see Col. 2 lines 41-43).

It would have been *prima facie* obvious to one of ordinary skill in the art at the time the invention was made to use the specific delay circuit 130 of Woods in place of the generic delay circuit 7 of Yoshimura for the purpose of having a simply constructed delay circuit that is used to delay the voltage of comparator 4, to prevent an erroneous output of the RESET signal. One skilled in the art would have been motivated to combine Yoshimura and Woods with a reasonable expectation of success.

With respect to claim 1, the above combination of Yoshimura and Woods, discloses, a detection circuit for monitoring a supply voltages the circuit comprising:

"a comparator (4 of Fig. 1 of Yoshimura) for generating a shortfall signal indicative of a shortfall of the supply voltage (VCC is supplied to 4 through 2) in relation to a reference voltage (5 supplies a reference voltage to 4, which is used with to Vcc to detect a shortfall in the supply voltage VCC.), and an integrator for time-integrating the shortfall signal to form an integrated signal (the modified delay circuit 7 now includes the resistor and capacitor of 130 of Fig. 1 of Woods. This resistor and capacitor arrangement integrates and delays the signal of comparator 4 being input to circuit 7), wherein the output of the integrator is used to generate a reset signal for resetting a microprocessor (the integrator circuit 7 is input to discriminator circuit 10, which uses both signals form 7 and 4 to output a reset signal, the resetting of the microprocessor is

deemed to be intended use, and the disclosed circuit provides the possibility of being used to reset a microprocessor.).”

With respect to claim 2, the above combination of Yoshimura and Woods discloses, a circuit according to claim 1 further including “a discriminator circuit for receiving the integrated signal (10 is a discriminator that receives the integrated signal c) and at least one further output of the comparator (it can be seen that 4 also additionally outputs a signal to circuit 10 at the node between 6 and 7), and generating a reset signal using the integrated signal and the at least one further output (10 uses both signals of the comparator and the integrated signal to output the reset signal e).”

With respect to claim 4, the above combination of Yoshimura and Woods discloses, “a comparator (4 of Fig. 1 of Yoshimura) for generating a shortfall signal indicative of a shortfall of the supply voltage (VCC is supplied to 4 through 2) in relation to a reference voltage (5 supplies a reference voltage to 4, which is used with to Vcc to detect a shortfall in the supply voltage VCC.), and an integrator for time-integrating the shortfall signal to form an integrated signal (the modified delay circuit 7 now includes the resistor and capacitor of 130 of Fig. 1 of Woods. This resistor and capacitor arrangement integrates and delays the signal of comparator 4 being input to circuit 7), wherein the output of the integrator is used to generate a reset signal for resetting a microprocessor (the integrator circuit 7 is input to discriminator circuit 10, which uses both signals form 7 and 4 to output a reset signal, the resetting of the microprocessor is deemed to be intended use, and the disclosed circuit provides the possibility of being used to reset a microprocessor.), and

reset means arranged to receive the reset signal outputted by the UVD circuit according to its value to initiate a reset of the microprocessor (Yoshimura discloses in Col. 1 lines 7-9, that the circuit can be used to monitor power supply for a voltage drop in an apparatus that needs back-up of data. It is obvious to one skilled in the art use Yoshimura's circuit to reset and detect a voltage drop in the supply voltage of a microprocessor, since they are known to be used to "back-up data". Thus it would be inherent that the microprocessor had a means to receive the reset signal, that is provided to it by Yoshimura's circuit.)."

With respect to claim 5, the above combination of Yoshimura and Woods discloses, "a method of monitoring a supply voltage including:

generating a shortfall signal indicative of a shortfall of the supply voltage in relation to a reference voltage (a shortfall signal is generated by 4 detecting when the Vcc drops below reference voltage 5); time-integrating the shortfall signal to form an integrated signal (the modified delay circuit 7 time integrates the output of 4 by low pass filtering the output of 4); and generating a reset signal using the shortfall signal, wherein the reset signal is for resetting a microprocessor (as explained above it would be obvious to use reset signal e, which is generated from the output signals of 4 and 7, to reset a microprocessor)."

With respect to claim 6, the above combination of Yoshimura and Woods discloses, the method of claim 5 and further comprising resetting the microprocessor with the reset signal (as stated above it would be obvious to use the reset signal e to reset a microprocessor)."

With respect to claim 7, the above combination with Yoshimura and Woods discloses, the circuit according to claim 4, wherein the UVD circuit further includes a discriminator circuit (10) for receiving the integrated signal (output of 7 c) and at least one further output of the comparator (output of 4 between the out of 6 and then input of 7), and generating a reset signal using the integrated signal and the at least one output (it can be seen that the RESET signal e is generated by 10, by receiving the signals output by 4 and 7) .

Allowable Subject Matter

Claim 8 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claim 3 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claim 3, there was no prior art found that taught the used of a control signal control switches of the discriminator circuit of Yoshimura. Also, there was no prior art found that provided motivation for combining Yoshimura with a switched discriminator that accepts signals output form a comparator, and an integrated signal that is generated form a different output of a comparator. Thus claim 3 is allowable, and claim 8 is allowed based on the same reasoning as claim 3.


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571) 272-5525. The examiner can normally be reached on Mondays - Fridays from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH
November 8, 2005


Terry D. Cunningham
Primary Examiner
Art Unit 2816